CLAIMS

1. A method comprising:

loading a value into a register of a memory device;

generating a test sequence in response to the value in the register during a self-test mode of operation of the memory device;

testing the memory device with the test sequence; and

storing a signature as a result of the test sequence into a shift register.

2. The method of claim 1 wherein the value is a four bit field.

3. The method of claim 1 wherein the memory device is a polymer memory organized as a 8K by 8K array with a 256 bit data word during the self-test mode of operation.

4. The method of claim 1 wherein the test sequence is one of a test pattern or a plurality of test patterns.

5. An article comprising:

a storage medium having a plurality of machine readable instructions, wherein when the instructions are executed by a memory device, the instructions provide to:

load a value into a register of the memory device;

generate a test sequence in response to the value in the register during a self-test mode of operation of the memory device;

test the memory device with the test sequence;

store a signature as a result of the test sequence into a shift register.

6. The article of claim 5 wherein the value is a four bit field.

7. The article of claim 5 wherein the memory device is a polymer memory organized as a 8K by 8K array with a 256 bit data word during the self-test mode of operation.

8. The article of claim 5 wherein the test sequence is one of a test pattern or a plurality of test patterns.

9. An apparatus to test a memory device comprising:

a register integrated within the memory device to load a value;

a logic to generate a test sequence in response to the value during a self-test mode of operation of the memory device and to test the memory device with the test sequence ;

a shift register to store a signature as a result of the test sequence; and

an error counter to tabulate the number of errors as the result of the test sequence.

10. The apparatus of claim 9 wherein the value is a four bit field.

11. The apparatus of claim 9 wherein the memory device is a polymer memory organized as a 8K by 8K array with a 256 bit data word during the self-test mode of operation.

12. The apparatus of claim 9 wherein the test sequence is one of a test pattern or a plurality of test patterns.

13. The apparatus of claim 9 wherein the error counter utilizes a shift register to tabulate the number of errors.

14. A memory device comprising:

a logic to support programmable built-in self-test (BIST) patterns; and

an error counter to tabulate a number of errors detected as a result of at least one BIST pattern applied to the memory device.

15. The memory device of claim 14 further comprising a plurality of programmable input data to test the memory device.

16. The memory device of claim 14 wherein at least one BIST pattern is to be generated by a data pattern stored in a chip test data register based at least in part on an address of the memory.

17. The memory device of claim 14 wherein the error counter is reset to zero before the BIST pattern is applied to the memory device.

18. The memory device of claim 14 wherein the error counter is incremented if the errors exceed a programmable threshold for an address of the memory device.

19. The memory device of claim 14 wherein the error counter is to count errors for a subset of the memory device, defined by a starting address and an ending address.

20. The memory device of claim 14 wherein the error counter is to count errors for a subset of a word, which represents a number of bits in an address.

21. The memory device of claim 14 wherein the error counter is a plurality of registers, the registers to store a count for at least one defect type and to store a count of the number of good bits for an address of the memory device.

22. The memory device of claim 21 wherein the defect type is either one of a stuck at one fault or a stuck at zero fault.